

FIGURE 1 (PRIOR ART)

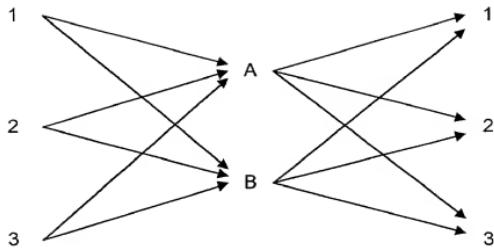


FIGURE 2 (PRIOR ART)

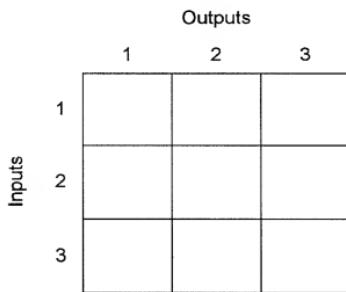


FIGURE 3 (PRIOR ART)

		Outputs		
		1	2	3
Inputs		1		A
		2		
Inputs		3		

FIGURE 4 (PRIOR ART)

		Outputs		
		1	2	3
Inputs		1		A
		2	A	
Inputs		3		B

FIGURE 5 (PRIOR ART)

		Outputs		
		1	2	3
Inputs		1		$\frac{A}{B}$
		2	$\frac{A}{B}$	
Inputs		3	A	B

FIGURE 6 (PRIOR ART)

Inputs

Switches

	A	B
1	3	
2	1	3
3		2

Outputs

Switches

	A	B
1	2	
2		3
3	1	2

FIGURE 7 (PRIOR ART)

Inputs

Switches

	A	B
1		3
2	1/3	3/1
3	1	2

Outputs

Switches

	A	B
1	2/3	2
2		3
3	1/2	2/1

FIGURE 8 (PRIOR ART)

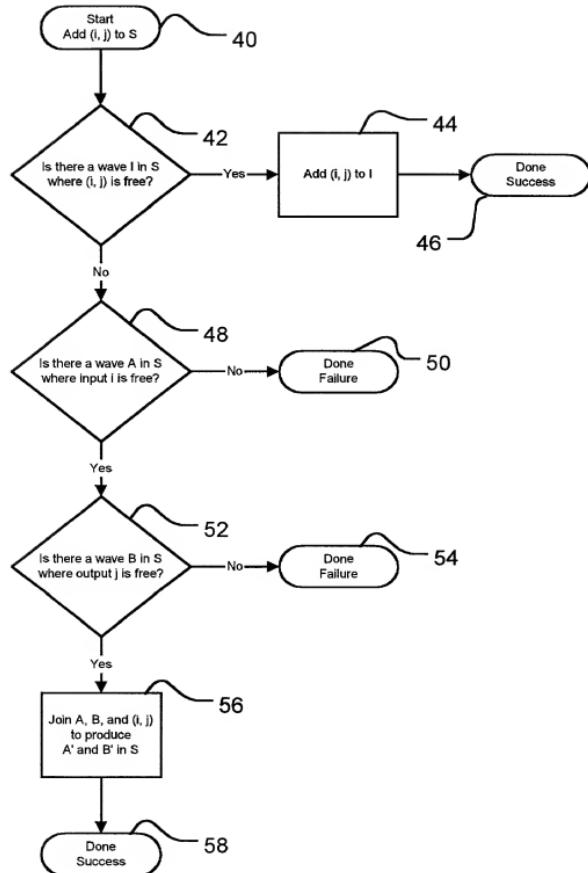


FIGURE 9

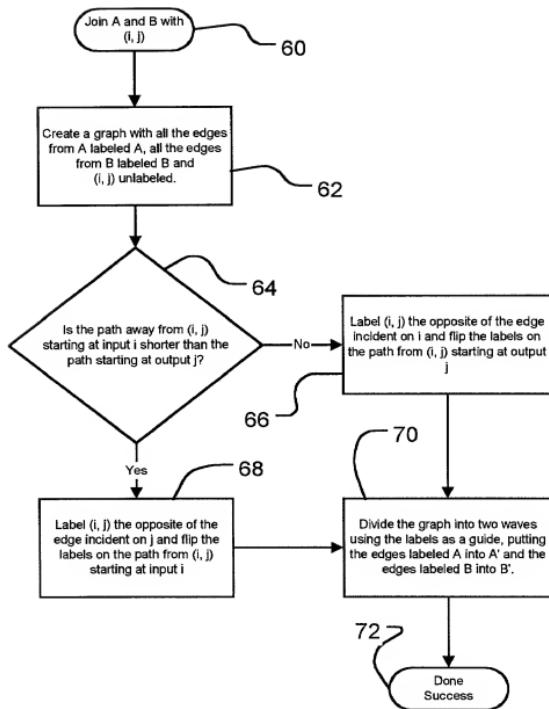


FIGURE 10

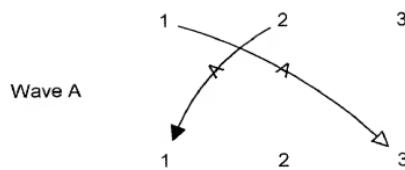


FIGURE 11

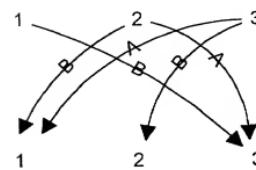
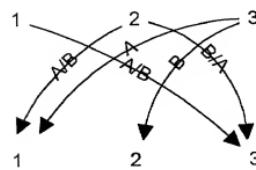
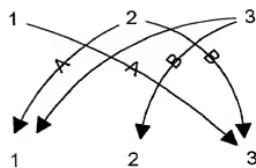


FIGURE 12

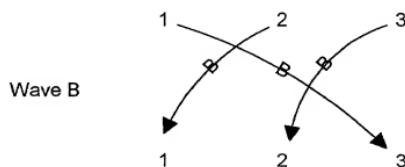
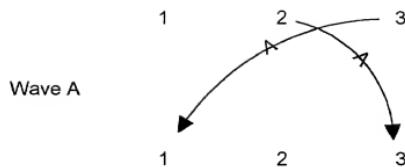


FIGURE 13

Switches		
	A B	
1	3	
2	1	3
3		2

Switches		
	A B	
1	2	
2		3
3	1	2

FIGURE 14

Switches		Switches	
	A		B
Inputs		3	
	1/3		3/1
	1	2	
Outputs		Outputs	
1	2/3	2	
2		3	
3	1/2	2/1	

FIGURE 15

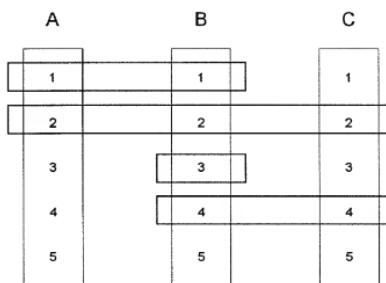


FIGURE 16